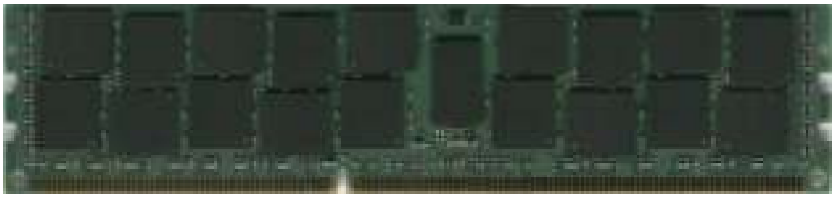
# DTM64385A

## 16GB - 240-Pin 2Rx4 Registered ECC DDR3 DIMM



**Identification**

DTM64385A 1Gx72

16GB 2Rx4 PC3-12800R-11-11-E2

**Performance range**

| Clock / Module Speed / CL-$t_{RCD}$ -$t_{RP}$ |
|---|
| 800 MHz / PC3-12800 / 11-11-11 |
| 667 MHz / PC3-10600 / 10-10-10 |
| 667 MHz / PC3-10600 / 9-9-9 |
| 533 MHz / PC3-8500 / 8-8-8 |
| 533 MHz / PC3-8500 / 7-7-7 |
| 400 MHz / PC3-6400 / 6-6-6 |

### Features

- 240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high
- Operating Voltage: 1.5V ±0.075
- I/O Type: SSTL_15
- On-board $I^2C$ temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 12.8 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 6, 7, 8, 9, 10, and 11
- Bi-directional Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 16/11/3
- Fully RoHS Compliant

### Description

DTM64385A is a registered 2Gx72 memory module, which conforms to JEDEC's DDR3, PC3-12800 standard. The assembly is Dual-Rank. Each Rank is comprised of eighteen Samsung 1Gx4 DDR3-1600 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

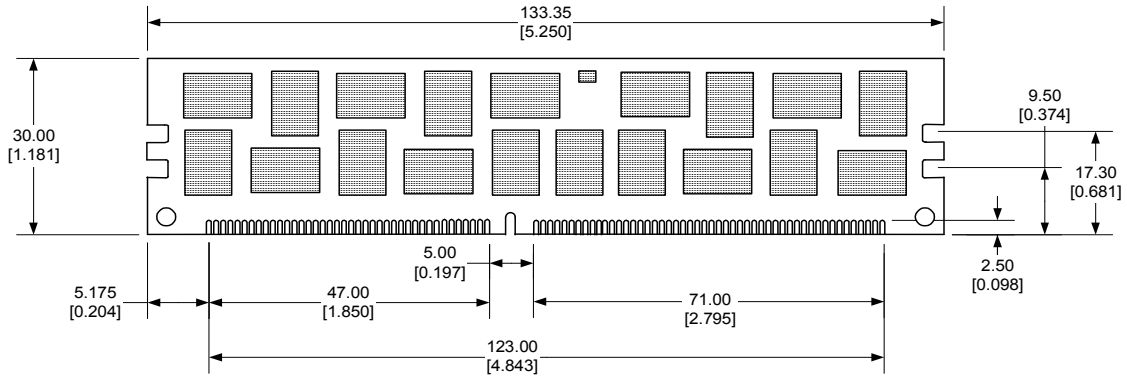
### Pin Configuration

| Front Side | | | | Back Side | | | |
|---|---|---|---|---|---|---|---|
| 1 $V_{REFDQ}$ | 31 DQ25 | 61 A2 | 91 DQ41 | 121 $V_{SS}$ | 151 $V_{SS}$ | 181 A1 | 211 $V_{SS}$ |
| 2 $V_{SS}$ | 32 $V_{SS}$ | 62 $V_{DD}$ | 92 $V_{SS}$ | 122 DQ4 | 152 DQS12 | 182 $V_{DD}$ | 212 DQS14 |
| 3 DQ0 | 33 /DQS3 | 63 CK1* | 93 /DQS5 | 123 DQ5 | 153 /DQS12 | 183 $V_{DD}$ | 213 /DQS14 |
| 4 DQ1 | 34 DQS3 | 64 /CK1* | 94 DQS5 | 124 $V_{SS}$ | 154 $V_{SS}$ | 184 CK0 | 214 $V_{SS}$ |
| 5 $V_{SS}$ | 35 $V_{SS}$ | 65 $V_{DD}$ | 95 $V_{SS}$ | 125 DQS9 | 155 DQ30 | 185 /CK0 | 215 DQ46 |
| 6 /DQS0 | 36 DQ26 | 66 $V_{DD}$ | 96 DQ42 | 126 /DQS9 | 156 DQ31 | 186 $V_{DD}$ | 216 DQ47 |
| 7 DQS0 | 37 DQ27 | 67 $V_{REFCA}$ | 97 DQ43 | 127 $V_{SS}$ | 157 $V_{SS}$ | 187 /EVENT | 217 $V_{SS}$ |
| 8 $V_{SS}$ | 38 $V_{SS}$ | 68 $P_{AR}_I_N$ | 98 $V_{SS}$ | 128 DQ6 | 158 CB4 | 188 A0 | 218 DQ52 |
| 9 DQ2 | 39 CB0 | 69 VDD | 99 DQ48 | 129 DQ7 | 159 CB5 | 189 $V_{DD}$ | 219 DQ53 |
| 10 DQ3 | 40 CB1 | 70 A10/AP | 100 DQ49 | 130 $V_{SS}$ | 160 $V_{SS}$ | 190 BA1 | 220 $V_{SS}$ |
| 11 $V_{SS}$ | 41 $V_{SS}$ | 71 BA0 | 101 $V_{SS}$ | 131 DQ12 | 161 DQS17 | 191 $V_{DD}$ | 221 DQS15 |
| 12 DQ8 | 42 /DQS8 | 72 $V_{DD}$ | 102 /DQS6 | 132 DQ13 | 162 /DQS17 | 192 /RAS | 222 /DQS15 |
| 13 DQ9 | 43 DQS8 | 73 /WE | 103 DQS6 | 133 $V_{SS}$ | 163 $V_{SS}$ | 193 /S0 | 223 $V_{SS}$ |
| 14 $V_{SS}$ | 44 $V_{SS}$ | 74 /CAS | 104 $V_{SS}$ | 134 DQS10 | 164 CB6 | 194 $V_{DD}$ | 224 DQ54 |
| 15 /DQS1 | 45 CB2 | 75 $V_{DD}$ | 105 DQ50 | 135 /DQS10 | 165 CB7 | 195 ODT0 | 225 DQ55 |
| 16 DQS1 | 46 CB3 | 76 /S1 | 106 DQ51 | 136 $V_{SS}$ | 166 $V_{SS}$ | 196 A13 | 226 $V_{SS}$ |
| 17 $V_{SS}$ | 47 $V_{SS}$ | 77 ODT1 | 107 $V_{SS}$ | 137 DQ14 | 167 NC (TEST) | 197 $V_{DD}$ | 227 DQ60 |
| 18 DQ10 | 48 $V_{TT}$ | 78 $V_{DD}$ | 108 DQ56 | 138 DQ15 | 168 /RESET | 198 /S3, NC | 228 DQ61 |
| 19 DQ11 | 49 $V_{TT}$ | 79 /S2, NC | 109 DQ57 | 139 $V_{SS}$ | 169 CKE1 | 199 $V_{SS}$ | 229 $V_{SS}$ |
| 20 $V_{SS}$ | 50 CKE0 | 80 $V_{SS}$ | 110 $V_{SS}$ | 140 DQ20 | 170 $V_{DD}$ | 200 DQ36 | 230 DQS16 |
| 21 DQ16 | 51 $V_{DD}$ | 81 DQ32 | 111 /DQS7 | 141 DQ21 | 171 A15 | 201 DQ37 | 231 /DQS16 |
| 22 DQ17 | 52 BA2 | 82 DQ33 | 112 DQS7 | 142 $V_{SS}$ | 172 A14 | 202 $V_{SS}$ | 232 $V_{SS}$ |
| 23 $V_{SS}$ | 53 $/E_{RR}_O_{UT}$ | 83 $V_{SS}$ | 113 $V_{SS}$ | 143 DQS11 | 173 $V_{DD}$ | 203 DQS13 | 233 DQ62 |
| 24 /DQS2 | 54 $V_{DD}$ | 84 /DQS4 | 114 DQ58 | 144 /DQS11 | 174 A12/BC | 204 /DQS13 | 234 DQ63 |
| 25 DQS2 | 55 A11 | 85 DQS4 | 115 DQ59 | 145 $V_{SS}$ | 175 A9 | 205 $V_{SS}$ | 235 $V_{SS}$ |
| 26 $V_{SS}$ | 56 A7 | 86 $V_{SS}$ | 116 $V_{SS}$ | 146 DQ22 | 176 $V_{DD}$ | 206 DQ38 | 236 $V_{DDSPD}$ |
| 27 DQ18 | 57 $V_{DD}$ | 87 DQ34 | 117 SA0 | 147 DQ23 | 177 A8 | 207 DQ39 | 237 SA1 |
| 28 DQ19 | 58 A5 | 88 DQ35 | 118 SCL | 148 $V_{SS}$ | 178 A6 | 208 $V_{SS}$ | 238 SDA |
| 29 $V_{SS}$ | 59 A4 | 89 $V_{SS}$ | 119 SA2 | 149 DQ28 | 179 $V_{DD}$ | 209 DQ44 | 239 $V_{SS}$ |
| 30 DQ24 | 60 $V_{DD}$ | 90 DQ40 | 120 $V_{TT}$ | 150 DQ29 | 180 A3 | 210 DQ45 | 240 $V_{TT}$ |

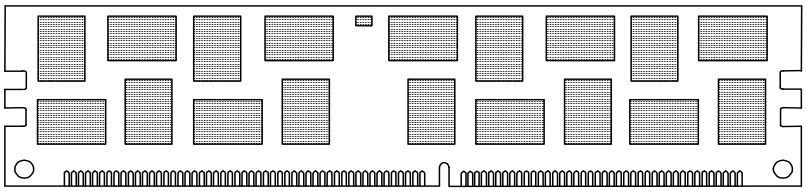
### Pin Description

| Name | Function |
|---|---|
| CB[7:0] | Data Check Bits |
| DQ[63:0] | Data Bits |
| DQS[17:0], /DQS[17:0] | Differential Data Strobes |
| CK[1:0], /CK[1:0] | Differential Clock Inputs |
| CKE[1:0] | Clock Enables |
| /CAS | Column Address Strobe |
| /RAS | Row Address Strobe |
| /S[3:0] | Chip Selects |
| /WE | Write Enable |
| A[15:0] | Address Inputs |
| BA[2:0] | Bank Addresses |
| ODT[1:0] | On Die Termination Inputs |
| SA[2:0] | SPD Address |
| SCL | SPD Clock Input |
| SDA | SPD Data Input/Output |
| /EVENT | Temperature Sensing |
| /RESET | Reset for register and DRAMs |
| PAR_IN | Parity bit for Addr/Ctrl |
| /ERR_OUT | Error bit for Parity Error |
| A12/BC | Combination input: Addr12/Burst Chop |
| A10/AP | Combination input: Addr10/Auto-precharge |
| $V_{SS}$ | Ground |
| $V_{DD}$ | Power |
| $V_{DDSPD}$ | SPD EEPROM Power |
| $V_{REFDQ}$ | Reference Voltage for DQ's |
| $V_{REFCA}$ | Reference Voltage for CA |
| $V_{TT}$ | Termination Voltage |
| NC | No Connection |
| | * not used |

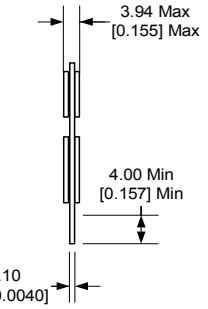
**Front view**




**Back view**



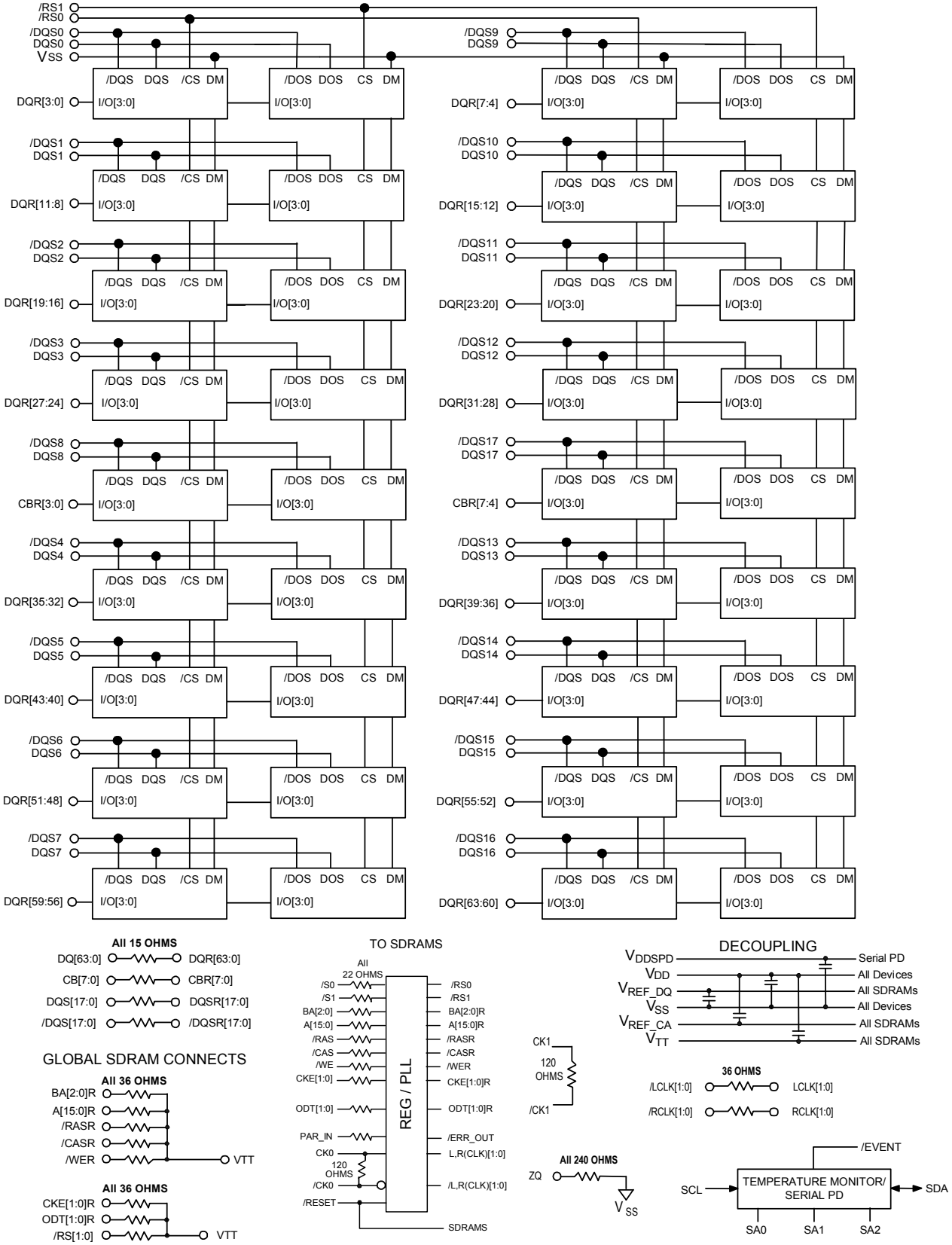
**Side view**




Notes

Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

All dimensions are expressed: millimeters [inches]


/RS1
/RS0
/DQS0
DQS0
VSS
/DQS9
DQS9
/DQS DQS /CS DM
/DOS DOS CS DM
I/O[3:0]
DQR[3:0]
DQR[7:4]
/DQS1
DQS1
/DQS10
DQS10
DQR[11:8]
DQR[15:12]
/DQS2
DQS2
/DQS11
DQS11
DQR[19:16]
DQR[23:20]
/DQS3
DQS3
/DQS12
DQS12
DQR[27:24]
DQR[31:28]
/DQS8
DQS8
/DQS17
DQS17
CBR[3:0]
CBR[7:4]
/DQS4
DQS4
/DQS13
DQS13
DQR[35:32]
DQR[39:36]
/DQS5
DQS5
/DQS14
DQS14
DQR[43:40]
DQR[47:44]
/DQS6
DQS6
/DQS15
DQS15
DQR[51:48]
DQR[55:52]
/DQS7
DQS7
/DQS16
DQS16
DQR[59:56]
DQR[63:60]


All 15 OHMS
DQ[63:0]
DQR[63:0]
CB[7:0]
CBR[7:0]
DQS[17:0]
DQSR[17:0]
/DQS[17:0]
/DQSR[17:0]


GLOBAL SDRAM CONNECTS
All 36 OHMS
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
VTT
All 36 OHMS
CKE[1:0]R
ODT[1:0]R
/RS[1:0]
VTT


TO SDRAMS
All
22 OHMS
/S0
/S1
BA[2:0]
A[15:0]
/RAS
/CAS
/WE
CKE[1:0]
ODT[1:0]
PAR_IN
CK0
120
OHMS
/CK0
/RESET
REG / PLL
/RS0
/RS1
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
CKE[1:0]R
ODT[1:0]R
/ERR_OUT
L,R(CLK)[1:0]
/L,R(CLK)[1:0]
SDRAMS


CK1
120
OHMS
/CK1


All 240 OHMS
ZQ
VSS


DECOUPLING
VDDSPD
Serial PD
VDD
All Devices
VREF_DQ
All SDRAMs
VSS
All Devices
VREF_CA
All SDRAMs
VTT
All SDRAMs


36 OHMS
/LCLK[1:0]
LCLK[1:0]
/RCLK[1:0]
RCLK[1:0]


/EVENT
SCL
TEMPERATURE MONITOR/
SERIAL PD
SDA
SA0
SA1
SA2

**Absolute Maximum Ratings**
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Temperature, non-Operating** | $T_{STORAGE}$ | -55 | 100 | C |
| **Ambient Temperature, Operating** | $T_A$ | 0 | 70 | C |
| **DRAM Case Temperature, Operating** | $T_{CASE}$ | 0 | 95 | C |
| **Voltage on $V_{DD}$ relative to $V_{SS}$** | $V_{DD}$ | -0.4 | 1.975 | V |
| **Voltage on Any Pin relative to $V_{SS}$** | $V_{IN}$,$V_{OUT}$ | -0.4 | 1.975 | V |

Notes:
DRAM Operating Case Temperature above 85C requires 2X refresh.

**Recommended DC Operating Conditions** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| **Power Supply Voltage** | $V_{DD}$ | 1.425 | 1.5 | 1.575 | V | |
| **SPD EEPROM Voltage** | VDDSPD | 3.0 | 3.3 | 3.6 | V | |
| **I/O Reference Voltage** | $V_{REFDQ}$ | 0.49 $V_{DD}$ | 0.50 $V_{DD}$ | 0.51 $V_{DD}$ | V | 1 |
| **I/O Reference Voltage** | $V_{REFCA}$ | 0.49 $V_{DD}$ | 0.50 $V_{DD}$ | 0.51 $V_{DD}$ | V | 1 |

Notes:
1) The value of $V_{REF}$ is expected to equal one-half $V_{DD}$ and to track variations in the $V_{DD}$ DC level. Peak-to-peak noise on $V_{REF}$ may not exceed ±1% of its DC value.

**DC Input Logic Levels, Single-Ended** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Logical High (Logic 1)** | $V_{IH(DC)}$ | $V_{REF}$ + 0.1 | $V_{DD}$ | V |
| **Logical Low (Logic 0)** | $V_{IL(DC)}$ | $V_{SS}$ | $V_{REF}$ - 0.1 | V |

**AC Input Logic Levels, Single-Ended** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Logical High (Logic 1)** | $V_{IH(AC)}$ | $V_{REF}$ + 0.175 | - | V |
| **Logical Low (Logic 0)** | $V_{IL(AC)}$ | - | $V_{REF}$ - 0.175 | V |

**Differential Input Logic Levels** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Differential Input Logic High** | $V_{IH.DIFF}$ | +0.200 | DC:$V_{DD}$ AC:$V_{DD}$+0.4 | V |
| **Differential Input Logic Low** | $V_{IL.DIFF}$ | DC:$V_{SS}$ AC:$V_{SS}$-0.4 | -0.200 | V |
| **Differential Input Cross Point Voltage relative to VDD/2** | $V_{IX}$ | - 0.150 | + 0.150 | V |

**Capacitance** ($T_A$ = 25 C, f = 100 MHz)

| PARAMETER | Pin | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| **Input Capacitance, Clock** | CK0, /CK0 | $C_{CK}$ | 1.5 | 2.5 | pF |
| **Input Capacitance, Address** | BA[2:0], A[15:0], /RAS, /CAS, /WE | $C_I$ | 1.5 | 2.5 | pF |
| **Input Capacitance Control** | /S[1:0], CKE[1:0], ODT[1:0] | $C_I$ | 1.5 | 2.5 | pF |
| **Input/Output Capacitance** | DQ[63:0], CB[7:0], DQS[17:0], /DQS[17:0]. | $C_{IO}$ | 3 | 5 | pF |

**DC Characteristics** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| **Input Leakage Current (Any input 0 V < VIN < VDD)** | $I_{IL}$ | -18 | +18 | µA | 1,2 |
| **Output Leakage Current (0V < VOUT < VDDQ)** | $I_{OL}$ | -10 | +10 | µA | 2,3 |

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ, DQS, DQS and ODT are disabled

**$I_{DD}$ Specifications and Conditions** ($T_A$ = 0 to 70 C, Voltage referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Test Condition | Max Value | Unit |
|---|---|---|---|---|
| **Operating One Bank Active-Precharge Current** | $I_{DD}0$* | Operating current : One bank ACTIVATE-to-PRECHARGE | 1900 | mA |
| **Operating One Bank Active-Read-Precharge Current** | $I_{DD}1$* | Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE | 2080 | mA |
| **Precharge Power-Down Current** | $I_{DD}2P$** | Precharge power down current: (Slow exit) | 770 | mA |
| **Precharge Power-Down Current** | $I_{DD}2P$** | Precharge power down current: (Fast exit) | 770 | mA |
| **Precharge Standby Current** | $I_{DD}2N$** | Precharge standby current | 1430 | mA |
| **Active Power-Down Current** | $I_{DD}3P$** | Active power-down current | 950 | mA |
| **Active Standby Current** | $I_{DD}3N$** | Active standby current | 1820 | mA |
| **Operating Burst Write Current** | $I_{DD}4W$* | Burst write operating current | 2800 | mA |
| **Operating Burst Read Current** | $I_{DD}4R$* | Burst read operating current | 2670 | mA |
| **Burst Refresh Current** | $I_{DD}5B$** | Refresh current | 3680 | mA |
| **Self Refresh Current** | $I_{DD}6$** | Self-refresh temperature current: MAX $T_C$ = 85°C | 550 | mA |
| **Operating Bank Interleave Read Current** | $I_{DD}7$* | All bank interleaved read current | 4080 | mA |

* One module rank in this operation, the rest in IDD2P slow exit.
** All module ranks in this operation.

## AC Operating Conditions

| PARAMETER | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Internal read command to first data | $t_{AA}$ | 13.125 | 20 | ns |
| CAS-to-CAS Command Delay | $t_{CCD}$ | 4 | - | $t_{CK}$ |
| Clock High Level Width | $t_{CH(avg)}$ | 0.47 | 0.53 | $t_{CK}$ |
| Clock Cycle Time | $t_{CK}$ | 1.25 | 2.500 | ns |
| Clock Low Level Width | $t_{CL(avg)}$ | 0.47 | 0.53 | $t_{CK}$ |
| Data Input Hold Time after DQS Strobe | $t_{DH}$ | 45 | - | ps |
| DQ Input Pulse Width | $t_{DIPW}$ | 360 | - | ps |
| DQS Output Access Time from Clock | $t_{DQSCK}$ | -225 | +225 | ps |
| Write DQS High Level Width | $t_{DQSH}$ | 0.45 | 0.55 | $t_{CK(avg)}$ |
| Write DQS Low Level Width | $t_{DQSL}$ | 0.45 | 0.55 | $t_{CK(avg)}$ |
| DQS-Out Edge to Data-Out Edge Skew | $t_{DQSQ}$ | - | 100 | ps |
| Data Input Setup Time Before DQS Strobe | $t_{DS}$ | 10 | - | ps |
| DQS Falling Edge from Clock, Hold Time | $t_{DSH}$ | 0.2 | - | $t_{CK(avg)}$ |
| DQS Falling Edge to Clock, Setup Time | $t_{DSS}$ | 0.2 | - | $t_{CK(avg)}$ |
| Clock Half Period | $t_{HP}$ | minimum of $t_{CH}$ or $t_{CL}$ | - | ns |
| Address and Command Hold Time after Clock | $t_{IH}$ | 120 | - | ps |
| Address and Command Setup Time before Clock | $t_{IS}$ | 45 | - | ps |
| Load Mode Command Cycle Time | $t_{MRD}$ | 4 | - | $t_{CK}$ |
| DQ-to-DQS Hold | $t_{QH}$ | 0.38 | - | $t_{CK(avg)}$ |
| Active-to-Precharge Time | $t_{RAS}$ | 35 | $9*t_{REFI}$ | ns |
| Active-to-Active / Auto Refresh Time | $t_{RC}$ | 48.125 | - | ns |
| RAS-to-CAS Delay | $t_{RCD}$ | 13.125 | - | ns |
| Average Periodic Refresh Interval $0^{o}$ C $\leq T_{CASE} < 85^{o}$ C | $t_{REFI}$ | - | 7.8 | µs |
| Average Periodic Refresh Interval $0^{o}$ C $\leq T_{CASE} < 95^{o}$ C | $t_{REFI}$ | - | 3.9 | µs |
| Auto Refresh Row Cycle Time | $t_{RFC}$ | 260 | - | ns |
| Row Precharge Time | $t_{RP}$ | 13.125 | - | ns |
| Read DQS Preamble Time | $t_{RPRE}$ | 0.9 | Note-1 | $t_{CK(avg)}$ |
| Read DQS Postamble Time | $t_{RPST}$ | 0.3 | Note-2 | $t_{CK(avg)}$ |
| Row Active to Row Active Delay | $t_{RRD}$ | Max(4nCK, 6ns) | - | ns |
| Internal Read to Precharge Command Delay | $t_{RTP}$ | Max(4nCK, 7.5ns) | - | ns |
| Write DQS Preamble Setup Time | $t_{WPRE}$ | 0.9 | - | $t_{CK(avg)}$ |
| Write DQS Postamble Time | $t_{WPST}$ | 0.3 | - | $t_{CK(avg)}$ |
| Write Recovery Time | $t_{WR}$ | 15 | - | ns |
| Internal Write to Read Command Delay | $t_{WTR}$ | Max(4nCK, 7.5ns) | - | ns |

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

## Serial Presence Detect

| Byte# | Function. | Value | Hex |
|---|---|---|---|
| 0 | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage. | | 0x92 |
| | Bit 3 ~ Bit 0. SPD Bytes Used - | 176 | |
| | Bit 6 ~ Bit 4. SPD Bytes Total - | 256 | |
| | Bit 7. CRC Coverage - | Bytes 0-116 | |
| 1 | SPD Revision. | Rev. 1.1 | 0x11 |
| 2 | Key Byte / DRAM Device Type. | DDR3 SDRAM | 0x0B |
| 3 | Key Byte / Module Type. | | 0x01 |
| | Bit 3 ~ Bit 0. Module Type - | RDIMM | |
| | Bit 7 ~ Bit 4. Reserved - | 0 | |
| 4 | SDRAM Density and Banks. | | 0x04 |
| | Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits - | 4Gb | |
| | Bit 6 ~ Bit 4. Bank Address Bits - | 8 banks | |
| | Bit 7. Reserved - | 0 | |
| 5 | SDRAM Addressing. | | 0x22 |
| | Bit 2 ~ Bit 0. Column Address Bits - | 11 | |
| | Bit 5 ~ Bit 3. Row Address Bits - | 16 | |
| | Bit 7, 6. Reserved | 0 | |
| 6 | Module Nominal Voltage, VDD. | | 0x00 |
| | Bit 0. NOT 1.5 V operable - | | |
| | Bit 1. 1.35 V operable - | | |
| | Bit 2. 1.2X V operable - | | |
| | Bit 3. Reserved - | | |
| | Bit 4. Reserved - | | |
| | Bit 5. Reserved - | | |
| | Bit 6. Reserved - | | |
| | Bit 7. Reserved - | | |
| 7 | Module Organization. | | 0x08 |
| | Bit 2 ~ Bit 0. SDRAM Device Width - | 4-Bits | |
| | Bit 5 ~ Bit 3. Number of Ranks - | 2-Rank | |
| | Bit 7, 6. Reserved | 0 | |
| 8 | Module Memory Bus Width. | | 0x0B |
| | Bit 2 ~ Bit 0. Primary bus width, in bits - | 64-Bits | |
| | Bit 4, Bit 3. Bus width extension, in bits - | 8-Bits | |
| | Bit 7 ~ Bit 5. Reserved - | 0 | |
| 9 | Fine Timebase (FTB) Dividend / Divisor. | | 0x11 |
| | Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor | 1 | |
| | Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend | 1 | |
| 10 | Medium Timebase (MTB) Dividend. | 1 (MTB = 0.125ns) | 0x01 |

| | | | |
|---|---|---|---|
| 11 | Medium Timebase (MTB) Divisor. | 8 (MTB = 0.125ns) | 0x08 |
| 12 | SDRAM Minimum Cycle Time (tCKmin). | 1.25ns | 0x0A |
| 13 | Reserved. | UNUSED | 0x00 |
| 14 | CAS Latencies Supported, Least Significant Byte. | | 0xFC |
| | Bit 0. CL = 4 - | | |
| | Bit 1. CL = 5 - | | |
| | Bit 2. CL = 6 - | X | |
| | Bit 3. CL = 7 - | X | |
| | Bit 4. CL = 8 - | X | |
| | Bit 5. CL = 9 - | X | |
| | Bit 6. CL = 10 - | X | |
| | Bit 7. CL = 11 - | X | |
| 15 | CAS Latencies Supported, Most Significant Byte. | | 0x00 |
| | Bit 0. CL = 12 - | | |
| | Bit 1. CL = 13 - | | |
| | Bit 2. CL =14 - | | |
| | Bit 3. CL = 15 - | | |
| | Bit 4. CL = 16 - | | |
| | Bit 5. CL = 17 - | | |
| | Bit 6. CL = 18 - | | |
| | Bit 7. Reserved. | | |
| 16 | Minimum CAS Latency Time (tAAmin). | 13.125ns | 0x69 |
| 17 | Minimum Write Recovery Time (tWRmin). | 15.0ns | 0x78 |
| 18 | Minimum RAS# to CAS# Delay Time (tRCDmin). | 13.125ns | 0x69 |
| 19 | Minimum Row Active to Row Active Delay Time (tRRDmin). | 6.0ns | 0x30 |
| 20 | Minimum Row Precharge Delay Time (tRPmin). | 13.125ns | 0x69 |
| 21 | Upper Nibbles for tRAS and tRC. | | 0x11 |
| | Bit 3 ~ Bit 0. tRAS Most Significant Nibble - | 1 | |
| | Bit 7 ~ Bit 4. tRC Most Significant Nibble - | 1 | |
| 22 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte. | 35.0ns | 0x18 |
| 23 | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte. | 48.125ns | 0x81 |
| 24 | Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte. | 260.0ns | 0x20 |
| 25 | Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte. | 260.0ns | 0x08 |
| 26 | Minimum Internal Write to Read Command Delay Time (tWTRmin). | 7.5ns | 0x3C |
| 27 | Minimum Internal Read to Precharge Command Delay Time (tRTPmin). | 7.5ns | 0x3C |
| 28 | Upper Nibble for tFAW. | | 0x00 |
| | Bit 3 ~ Bit 0. tFAW Most Significant Nibble - | 0 | |
| | Bit 7 ~ Bit 4. Reserved - | 0 | |

| | | | |
|---|---|---|---|
| 29 | Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte. | 30.0ns | 0xF0 |
| 30 | SDRAM Optional Features. | | 0x83 |
| | Bit 0. RZQ / 6 - | X | |
| | Bit 1. RZQ / 7 - | X | |
| | Bit 6 ~ Bit 2. Reserved - | | |
| | Bit 7. DLL-Off Mode Support | | |
| 31 | SDRAM Drivers Supported. | | 0x01 |
| | Extended Temperature Range - | X | |
| | Extended Temperature Refresh Rate - | | |
| | Auto Self Refresh (ASR) - | | |
| | On-die Thermal Sensor (ODTS) Readout - | | |
| | Reserved - | | |
| | Reserved - | | |
| | Reserved - | | |
| | Partial Array Self Refresh (PASR) - | | |
| 32 | Module Thermal Sensor. | | 0x80 |
| | Bit 6 ~ Bit 0. Thermal Sensor Accuracy - | 0 | |
| | Bit 7. Thermal Sensor - | With TS | |
| 33 | SDRAM Device Type. | | 0x00 |
| | Bit 6 ~ Bit 0. Non-Standard Device Description - | 0 | |
| | Bit 7. SDRAM Device Type - | Std Mono | |
| 34 -59 | Reserved | UNUSED | 0x00 |
| 60 | Module Nominal Height. | | 0x0F |
| | Bit 4 ~ Bit 0. Module Nominal Height max, in mm - | 29<h<=30 | |
| | Bit 7 ~ Bit5. Reserved - | 0 | |
| 61 | Module Maximum Thickness. | | 0x11 |
| | Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) - | 1<th<=2 | |
| | Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) - | 1<th<=2 | |
| 62 | Reference Raw Card Used. | | 0x44 |
| | Bit 4 ~ Bit 0. Reference Raw Card - | R/C E | |
| | Bit 6, Bit 5. Reference Raw Card Revision - | Rev.2 | |
| | Bit 7. Reserved - | 0 | |
| 63 | (Registered) DIMM Module Attributes. | | 0x09 |
| | Bit 1 ~ Bit 0. # of Registers used on RDIMM - | 1 Register | |
| | Bit 3 ~ Bit 2. # of Rows of DRAMs on RDIMM - | 2 Rows | |
| | Bit 7 ~ Bit 4. Reserved - | 0 | |
| 64 | RDIMM Thermal Heat Spreader Solution. | | 0x00 |
| | Bit 6 ~ Bit 0. Heat Spreader Thermal Characteristics - | 0 | |
| | Bit 7. Heat Spreader Solution - | No HS | |
| 65 | Register Manufacturer ID Code, Least Significant Byte (Optional). | | 0x80 |

| | | | |
|---|---|---|---|
| 66 | Register Manufacturer ID Code, Most Significant Byte (Optional). | | 0xB3 |
| 67 | Register Revision Number (Optional). | | 0x63 |
| 68 | Register Type. | | 0x00 |
| | Bit[2-0] Support Device - | SSTE32882 | |
| | Bit[7-3] Reserved - | 0 | |
| 69 | [SSTE32882]: RC1 (MS Nibble) / RC0 (LS Nibble) | UNUSED | 0x00 |
| 70 | [SSTE32882]: RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address. | | 0x50 |
| | Bit 1, Bit 0. RC2/DA3,4 Value.- | RESERVED | |
| | Bit 3, Bit 2. RC2/DBA0,1 Value - | RESERVED | |
| | Bit 5, Bit 4. RC3/DA4,3 value, Command/Address A Outputs - | Moderate | |
| | Bit 7, Bit 6. RC3/DBA0,1 value, Command/Address B Outputs - | Moderate | |
| 71 | [SSTE32882]: RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock. | | 0x55 |
| | Bit 1, Bit 0. RC4/DA3,4 Control Signals, A Outputs.- | Moderate | |
| | Bit 3, Bit 2. RC4/DBA0,1 Control Signals, B Outputs - | Moderate | |
| | Bit 5, Bit 4. RC5/DA4,3 value, Y1/Y1# and Y3/Y3# Clock Outputs - | Moderate | |
| | Bit 7, Bit 6. RC5/DBA0,1 value, Y0/Y0# and Y2/Y2# Clock Outputs - | Moderate | |
| 72 | [SSTE32882]: RC7 (MS Nibble) / RC6 (LS Nibble). | UNUSED | 0x00 |
| 73 | [SSTE32882]: RC9 (MS Nibble) / RC8 (LS Nibble). | UNUSED | 0x00 |
| 74 | [SSTE32882]: RC11 (MS Nibble) / RC10 (LS Nibble). | UNUSED | 0x00 |
| 75 | [SSTE32882]: RC13 (MS Nibble) / RC12 (LS Nibble). | UNUSED | 0x00 |
| 76 | [SSTE32882]: RC15 (MS Nibble) / RC14 (LS Nibble). | UNUSED | 0x00 |
| 77-112 | Module-Specific Section | UNUSED | 0x00 |
| 113 | Module-Specific Section. | UNUSED | 0x00 |
| 114-116 | Module-Specific Section | UNUSED | 0x00 |
| 117 | Module Manufacturer ID Code, Least Significant Byte | | 0x80 |
| 118 | Module Manufacturer ID Code, Most Significant Byte | | 0xCE |
| 119 | Module Manufacturing Location | | 0x01 |
| 120 | Module Manufacturing Date | | 0x11 |
| 121 | Module Manufacturing Date | | 0x37 |
| 122 | Module Serial Number | | 0x44 |
| 123 | Module Serial Number | | 0x32 |
| 124 | Module Serial Number | | 0xC4 |
| 125 | Module Serial Number | | 0xF8 |
| 126 | Cyclical Redundancy Code (CRC). | CRC | 0x34 |
| 127 | Cyclical Redundancy Code (CRC). | CRC | 0x22 |
| 128 | Module Part Number | M | 0x4D |

| | | | |
|---|---|---|---|
| 129 | Module Part Number | 3 | 0x33 |
| 130 | Module Part Number | 9 | 0x39 |
| 131 | Module Part Number | 3 | 0x33 |
| 132 | Module Part Number | B | 0x42 |
| 133 | Module Part Number | 2 | 0x32 |
| 134 | Module Part Number | G | 0x47 |
| 135 | Module Part Number | 7 | 0x37 |
| 136 | Module Part Number | 0 | 0x30 |
| 137 | Module Part Number | B | 0x42 |
| 138 | Module Part Number | H | 0x48 |
| 139 | Module Part Number | 0 | 0x30 |
| 140 | Module Part Number | - | 0x2D |
| 141 | Module Part Number | C | 0x43 |
| 142 | Module Part Number | K | 0x4B |
| 143 | Module Part Number | 0 | 0x30 |
| 144, 145 | Module Part Number | | 0x20 |
| 146, 147 | Module Revision Code | UNUSED | 0x00 |
| 148 | DRAM Manufacturer ID Code, Least Significant Byte | | 0x80 |
| 149 | DRAM Manufacturer ID Code, Most Significant Byte | | 0xCE |
| 150-175 | Manufacturer's Specific Data | UNUSED | 0x00 |
| 176-255 | Open for customer use | UNUSED | 0x00 |

Note: Bytes 119 – 125 and 150 - 255 may be different than shown.

DATARAM CORPORATION, USA Corporate Headquarters, P.O. Box 7528, Princeton, NJ 08543-7528;
Voice: 609-799-0071, Fax: 609-799-6734; www.dataram.com

All rights reserved.

The information contained in this document has been carefully checked and is believed to be reliable. However, Dataram assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Dataram.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Dataram.